JOURNAL OF SPACECRAFT AND ROCKETS
Vol. 30, No. 3, May–June 1993

Monolithic V-Band High-Electron Mobility Transistor Downconverter Component Development for Satellite Communication Links

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This paper presents the design and performance of a complete monolithic downconverter developed for satellite communication links using high electron mobility transistor technology. Individual components, including V-band amplifiers, a V-band mixer, and a 2–10 GHz intermediate frequency amplifier, were designed, fabricated, and tested. The monolithic downconverter demonstrated a measured conversion gain of 22 dB at 60 GHz rf frequency with a local oscillator drive of +10 mW at 54 GHz, which represents state-of-the-art performance for highly integrated monolithic millimeter-wave integrated circuits at this frequency.

I. Introduction

V-BAND downconverters are important subsystems in the receiving chain of satellite communication systems. In present satellite-based communications, it is necessary to maximize data throughput, increase coverage areas, minimize dependence on ground stations, and reduce the probability of intercept and jamming capabilities. The use of 60 GHz as a communication link frequency is desired because of the low probability of intercept from the ground, as well as the significant bandwidth capability with reasonable size and weight constraints. Wide-scale implementation of 60 GHz communication links in the future depends on the availability of small, lightweight, and inexpensive millimeter-wave (MMW) monolithic integrated circuit (IC) components.

The high electron mobility transistor (HEMT) has demonstrated high-gain and low-noise capability in MMW frequency components. Several V-band monolithic low-noise amplifiers (LNAs) using HEMT technology have been reported[1–3] as well as a V-band diode mixer using a metal semiconductor field effect transistor compatible process.[4] The recent refinements of HEMT technology make it possible to achieve a high level of integration for MMW monolithic ICs, allowing a monolithic V-band downconverter to be developed using 0.2 μm T gate (or mushroom gate, describing the shape of Schottky gate profile in the transistor) InGaAs/GaAs pseudomorphic HEMT technology. The downconverter components consist of two V-band rf LNAs, a singly balanced diode downconverting mixer, and a distributed intermediate frequency (IF) amplifier. The monolithic downconverter demonstrated a conversion gain of 22 dB when downconverting a signal of 60 to 6 GHz with a local oscillator (LO) drive of 10 mW at 54 GHz. The individual components were also fabricated on the same wafer and tested. A rigorous design/analysis methodology was incorporated in the monolithic chip development, which includes accurate device modeling and full-wave electromagnetic (EM) analysis of passive structures. The success of this chip development is attributed to the stable HEMT processing technology and the rigorous design methodology. Section II discusses the design/modeling methodology for MMW monolithic ICs, and Sec. III describes the individual components and downconverter designs. The 0.2 μm T-gate InGaAs/GaAs pseudomorphic HEMT monolithic microwave integrated circuit process and fabrication is presented in Sec. IV. Section V contains measurement data and is followed by a brief summary.

II. Design/Modeling Methodology for MMW Monolithic ICs

The design/analysis methodology that was applied to the monolithic chip development includes accurate device modeling and full-wave EM analysis of passive structures. It is similar to the W-band monolithic LNA design reported previously[5] and is described here briefly.

A. Active and Passive Elements Modeling

Both accurate HEMT device modeling and passive structure analysis are very important for the MMW monolithic IC design. The HEMT device linear model was obtained by fitting measured *S* parameters to 40 GHz, whereas the noise model was generated from measured noise parameters to 26 GHz. The dc I-V curves were used for the device nonlinear characterization. Once the accurate low-frequency model was developed, performance could be extrapolated to the band of interest.

There are concerns about passive structure model inconsistencies between MMW and microwave frequencies for monolithic IC design. The validity of models, which are generated by quasistatic analysis or empirical formula[6,7] and are widely used in most microwave circuit theory based computer-aided design (CAD) programs, should be further investigated. Also, additional care should be exercised when applying microwave circuit theory to high-frequency structures since the coupling effect between elements tends to be stronger at high frequencies. The numerical full-wave EM analysis to characterize arbitrarily shaped passive structures is preferred.

Several full-wave EM analysis tools are commercially available based on different approaches using different physical assumptions or numerical techniques. These approaches include the method of moments to solve various integral equations and the finite element method to solve partial differential equations (Maxwell's equations). Based on the calculated surface current or field distribution,

Received Feb. 6, 1992; presented as Paper 92-1906 at the AIAA 14th International Communications Satellite Systems Conference, Washington, DC, March 22–26, 1992; revision received Sept. 12, 1992; accepted for publication Sept. 23, 1992.

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any particular passive structure can be characterized in terms of the *S*-parameters, which are suitable for circuit design. The EM analysis being used in our design is a method of moments solution for the surface current integral equation based on the assumption of a stratified medium in a conducting box.[8]

B. Design/Analysis Procedure

The computation time of full-wave EM analysis in the design cycle is a concern. Currently, most microwave circuit theory based CAD tools allows optimization to fine tune the circuit performance. However, optimization of circuit performance using EM analysis is not practical at present due to the amount of time the optimization requires. To use the tools more efficiently, a design/analysis procedure was developed.

After accurate device modeling has been completed, conventional circuit synthesis and simulation using existing models of passive elements are performed for the initial design. The critical components, for which the models are suspect, are identified and characterized by EM analysis. The design is then modified based on resimulation using the EM analysis results. After the design is complete, the entire matching structure is analyzed by EM theory to insure no severe coupling effects between elements. If there is significant impact on the circuit performance, more complicated critical components need to be defined and the design/analysis procedure is repeated.

III. Monolithic Components and Downconverter Design

The V-band receiver block diagram developed for communication links is illustrated in Fig. 1. The shaded area indicates the recently developed monolithic downconverter. This monolithic unit integrates two 60 GHz two-stage LNAs, a V-band singly balanced diode mixer, and a 2-10 GHz IF LNA. The front end 60 GHz

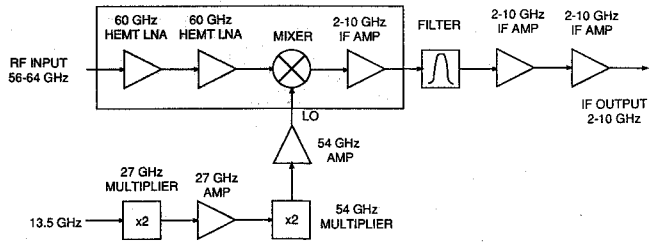


Fig. 1 Block digram of the V-band receiving system.

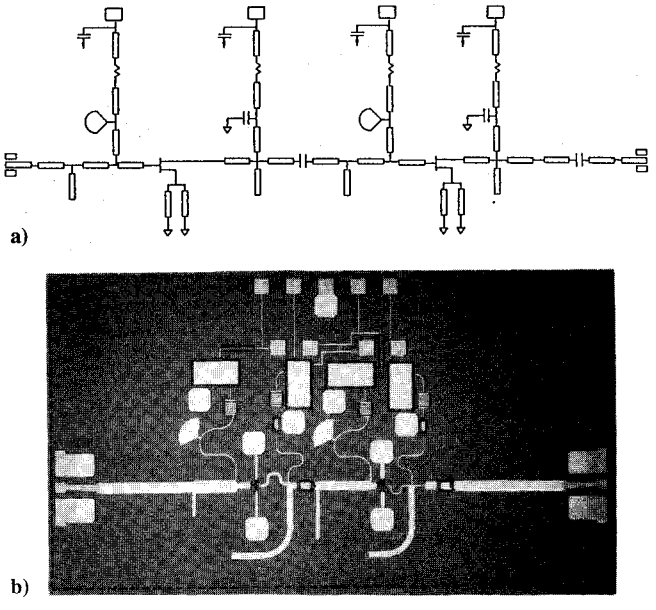


Fig. 2 a) Circuit schematic diagram, and b) chip photograph of the monolithic V-band LNA.

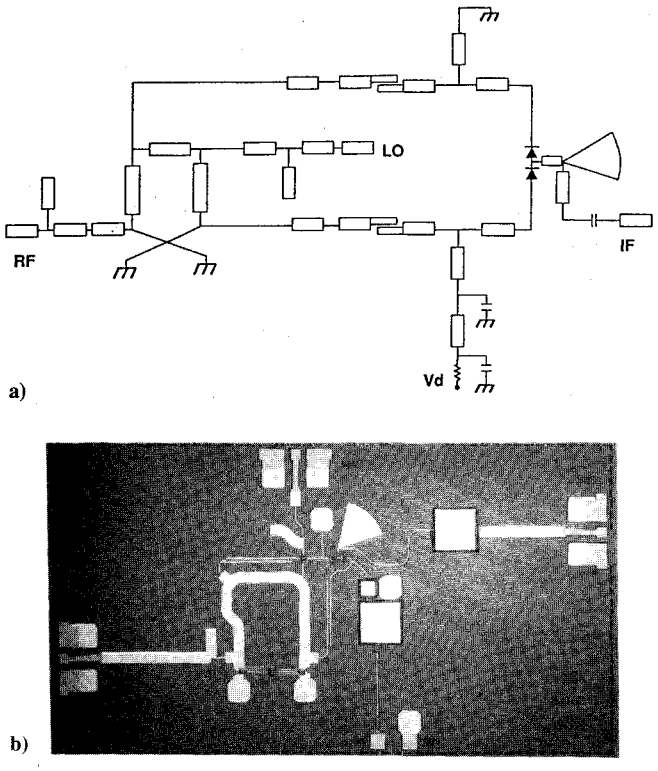


Fig. 3 a) Circuit schematic diagram, and b) chip photograph of the monolithic singly balanced diode mixer.

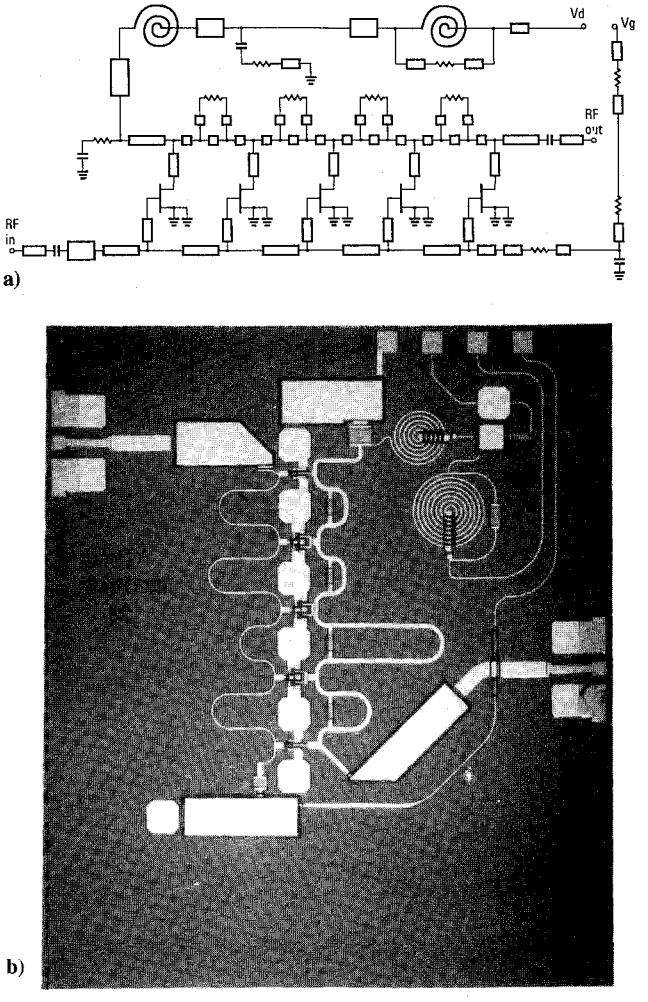


Fig. 4 a) Circuit schematic diagram, and b) chip photograph of the monolithic distributed IF amplifier.

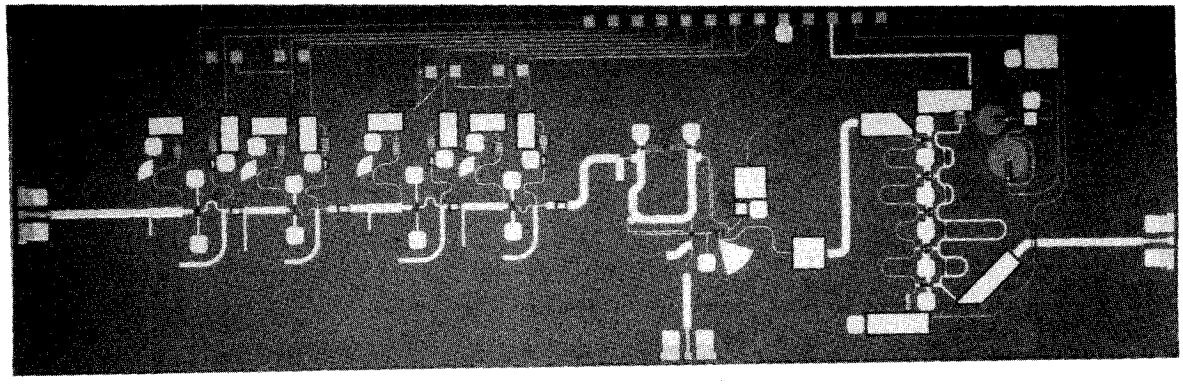
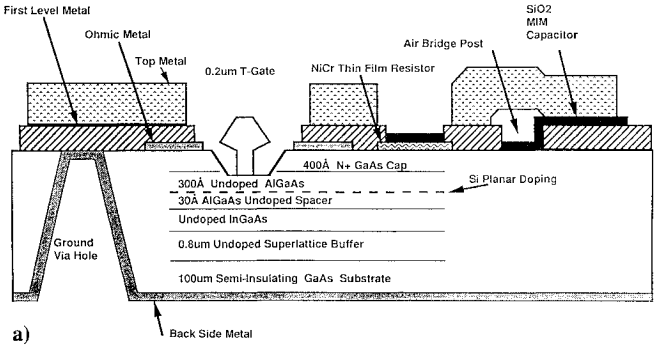
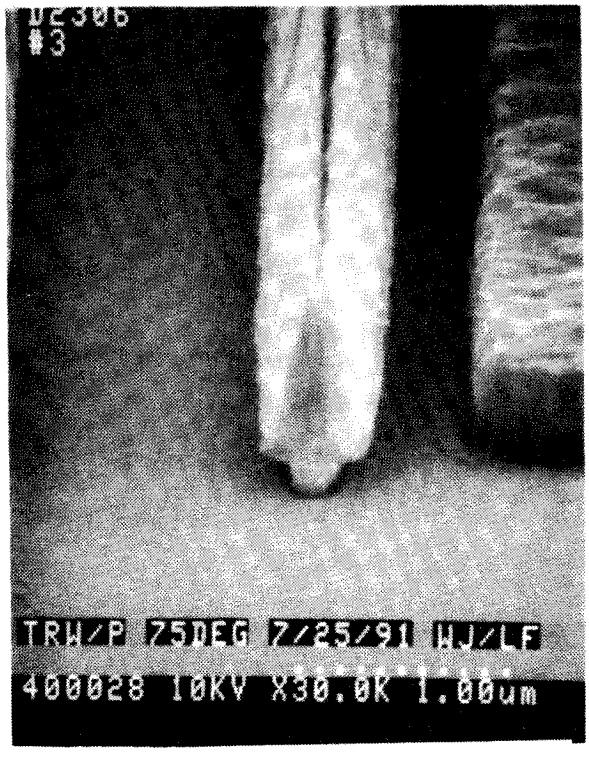


Fig. 5 Chip photograph of the monolithic downconverter.



a)



b)

Fig. 6 a) The 0.2 μm InGaAs/GaAs HEMT layer structure, and b) the scanning electron microscope photograph of the 0.2 μm T-shaped gate.

two-stage LNAs are mainly for low-noise figure consideration of the complete downconverter chip. The singly balanced design approach is chosen for the mixer to achieve the in-band even-order spurious signal rejection and good port-to-port isolation. The IF output of the downconverter is passed through band-limiting filters and two monolithic postamplifiers.

All of the monolithic circuits are fabricated using the 0.2 μm T-gate HEMT process on a 76.2-mm-diam GaAs wafer thinned down to 100 μm. Both linear and nonlinear circuit simulations were performed during the design to predict the circuit performance. The individual circuit and downconverter designs are described as follows.

A. V-Band Monolithic LNA

The V-band LNA is a two-stage single-ended design similar to the one reported earlier.[2] The circuit schematic diagram and photograph of the chip are shown in Fig. 2. Each stage used a 40 μm gate-width HEMT with four gate fingers. The matching circuits are composed of series transmission lines, open stubs, and metal-insulated metal (MIM) capacitors. The radial stubs and shunt MIM capacitors were used as rf grounds in the gate and drain bias networks. MIM capacitors were used for the interstage dc blocks. The on-chip bias networks were carefully designed for unconditional stability. The chip size is 3.6×2.0 mm^2.

B. Singly Balanced Diode Mixer

The frequency downconverting mixer is a singly balanced design using two diodes. Figure 3 illustrates the circuit schematic diagram and chip photograph. The chip size is 3.6×2.0 mm^2. It converts a V-band rf signal to a 2–10 GHz IF signal using an LO frequency centered at 54 GHz. The Schottky gate diode is formed by connecting the drain and source terminals of an HEMT as the anode. The modified rat-race[9] 3 dB coupler that provides wide bandwidth is chosen as the balun (balance to unbalance transformer). Since the modified rat race is a 180-deg balun, this mixer can also be used as a frequency upconverter.[10]

C. Distributed IF Amplifier

The 2–10 GHz IF amplifier uses a five-cell distributed architecture to achieve wide bandwidth. The design is similar to the one reported previously.[11] Both 90 and 120 μm HEMTs are used in the design. The distributed amplifier was optimized for broadband low-noise performance. The circuit schematic diagram and chip photograph are shown in Fig. 4. The chip size is 2.6×3.0 mm^2.

D. Downconverter Design

The downconverter is constructed by cascading two V-band LNAs as the front end, followed by the downconverting mixer. The mixer output is connected to the input of the IF amplifier. Since each component is matched to a 50 Ω environment, 50 Ω transmission lines are used to join the circuits. A photograph of the monolithic downconverter is shown in Fig. 5. The chip size is 9.6×3.0 mm^2.

IV. Fabrication of Monolithic Circuits

The fabrication for the circuits was performed on pseudomorphic InGaAs/GaAs HEMT material grown on a 76.2-mm-diam undoped GaAs substrate using a Varian Generation II modular molecular beam epitaxial system. The high mobility and sheet density result in higher transconductance and thus higher cutoff frequency capabilities for devices and circuits compared to the lattice-matched AlGaAs/GaAs HEMT structure.[12] The InGaAs/GaAs HEMT layer structure shown in Fig. 6a consisted of a GaAs/

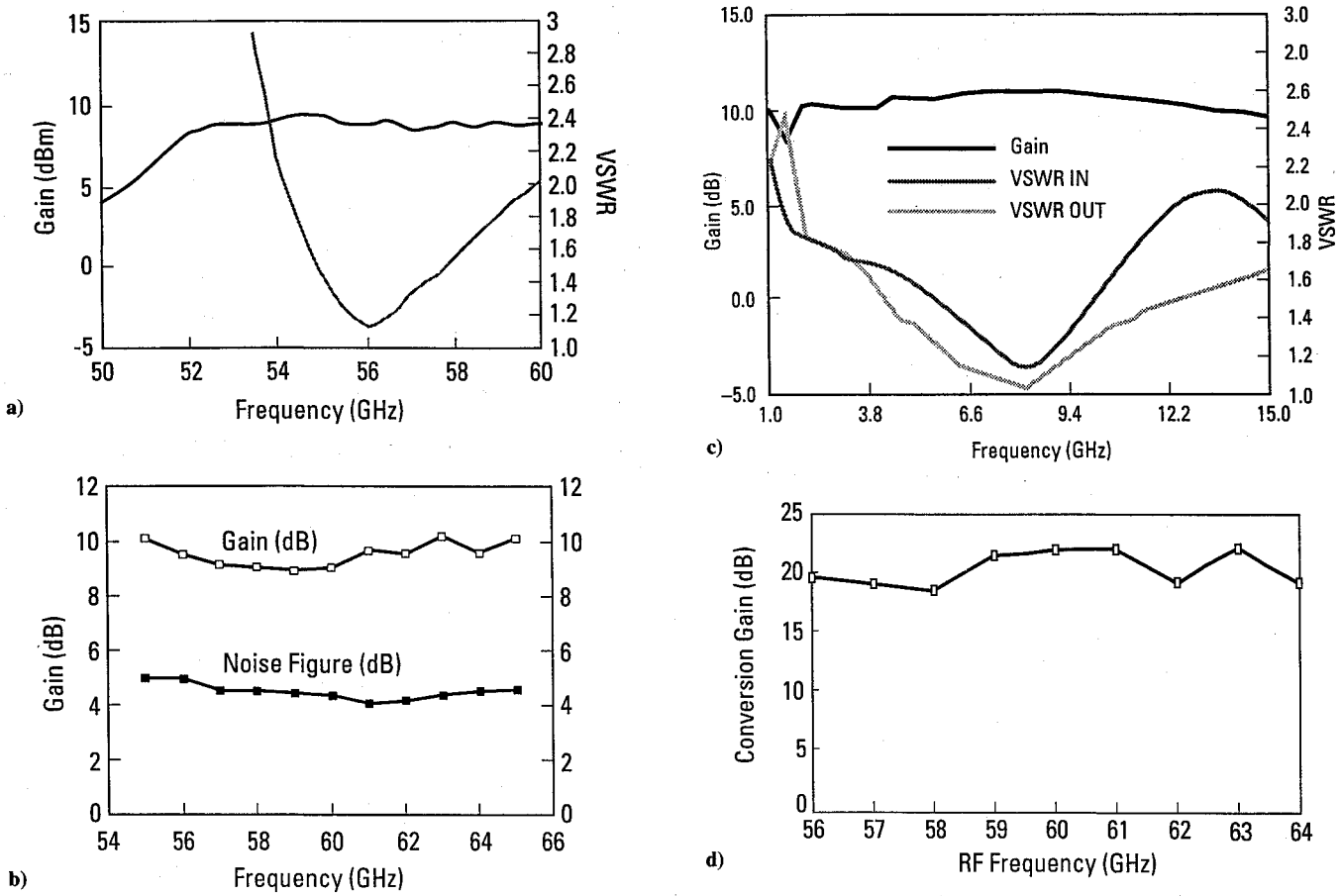


Fig. 7 Measurement results for a) the small signal gain and input VSWR of the V-band LNA, b) NF and associated gain of the V-band LNA, c) gain and VSWR of the distributed IF amplifier, and d) conversion gain of the monolithic downconverter.

AlGaAs superlattice buffer, an undoped InGaAs channel, a 0.003 μm AlGaAs spacer layer, a planar-doped monolayer of silicon, a 0.03 μm undoped layer of AlGaAs, and a 0.04 μm layer of N^+ GaAs for the cap to aid in the reduction of the ohmic contact resistance.

The HEMT monolithic IC process includes a multiple oxygen implant to isolate the active regions, an AuGe metalization for the source-drain ohmic contact that is thermally annealed rapidly to insure good ohmic contact, nichrome for thin film resistors, a low-temperature silicon dioxide layer for the MIM capacitor, first level interconnect metal and top metal to form transmission lines, and top plates for capacitors and inductors. The 0.2 μm T-shaped gate depicted by the scanning electron microscope photograph in Fig. 6b is formed using a Philips electron beam lithography system to write the gate pattern with a polymethyl methacrylate/copolymers methyl methacrylate and methacrylate acide [PMMA/P(MMA-MAA)] bilevel resist structure. The opening in the PMMA is used to recess the device to achieve a current level that will insure device pinch off, minimum noise figure, and maximum associated gain at a low-power bias condition. The monolithic circuits are completed by thinning the wafer down to 100 μm before etching back side via holes and plating up to 3 μm of Au to interconnect the source grounds. Extensive in-process monitoring is implemented to insure a reproducible, high-yield process from wafer to wafer.

V. Measured Performance

On-wafer rf probing techniques were used to measure the gain and voltage standing wave ratio (VSWR) performance for all of the circuits. The V-band LNA exhibited a measured gain of 9 dB and an input VSWR better than 2.3 from 54 to 60 GHz as shown in Fig. 7a. The noise figure and associated gain measurement of the V-band LNA from 56 to 64 GHz in a test fixture are depicted in Fig. 7b. It shows a noise figure of 4.5 dB. The IF amplifier demonstrated a gain of 11 dB with input and output VSWR better than 1.8 from 2 to 10 GHz as indicated in Fig. 7c. The downconverting mixer showed a measured conversion loss of 8 dB when injecting an rf signal at 60 GHz with an LO drive of +10 mW at 54 GHz and a 1.2 V bias voltage. The complete downconverter gain is shown in Fig. 7d. The 20±2 dB conversion gain was measured with an rf signal from 56 to 64 GHz and a fixed LO drive of +10 dBm at 54 GHz. The noise figure of the downconverter chip is estimated to be 5–7 dB based on the noise figure performance of the preamplifier.

VI. Summary

We have presented the recent development of a V-band monolithic downconverter using 0.2 μm pseudomorphic HEMT technology. The monolithic downconverter demonstrated a measured conversion gain of 22 dB at 60 GHz rf frequency with an LO drive of +10 dBm at 54 GHz. These results represent state-of-the-art performance for high-level integration of MMW monolithic ICs at this frequency and make this monolithic downconverter chip ideal for satellite communication link applications. The stable monolithic IC processing technology and rigorous design/analysis methodology are the foundations of this successful V-band monolithic IC development.

Acknowledgments

The authors would like to thank H. Berger and J. Maguire for their support of this project, B. Allen for his technical inputs, D. Streit for molecular beam epitaxial material growth support, P. Liu for T-gate lithography assistance, W. Bartolome for his layout help, F. Oshita and D. Brunone for testing efforts, and L. Liu, W. Lam, H. L. Wiedersphan, and J. Yonaki for their discussions and suggestions.

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Associate Editor